



## COURSE PRESENTATION FORM – ACADEMIC YEAR 2010/2011

<b>COURSE NAME</b>	<b>Formal Methods</b>
<b>COURSE CODE</b>	72049 (MSc New – DM 270) / 70144 (BSc + MSc Old – DM 509) / 70058 (BSc Old)
<b>LECTURER</b>	<a href="#">Alessandro Artale</a>
<b>TEACHING ASSISTANTS</b>	<a href="#">Enrico Franconi</a>
<b>TEACHING LANGUAGE</b>	English
<b>CREDIT POINTS</b>	4
<b>LECTURE HOURS</b>	24
<b>EXERCISE HOURS</b>	12
<b>TIME SPAN</b>	27.09.2010 - 21.01.2011
<b>TIME TABLE</b>	See <a href="#">Timetable Page</a>
<b>OFFICE HOURS LECTURER</b>	During the lecture time, Wednesday from 16:00 to 18:00, <a href="#">Faculty of CS, POS Building, piazza Domenicani 3</a> , office 2.03
<b>OFFICE HOURS TEACHING ASSISTANT</b>	During the lecture time, TBD, <a href="#">Faculty of CS, POS Building, piazza Domenicani 3</a> , office 3.06
<b>PREREQUISITES</b>	Courses: Logic
<b>OBJECTIVES</b>	<p>In this module students will develop a deeper understanding of technologies based on applying formal methods for the specification and verification of hardware systems.</p> <p>Students will learn the most important techniques based on Model Checking to check properties of a system.</p> <p>In particular, the student will be able to understand how to formally specify a hardware system by means of transition systems and how to express computation properties by means of formulas in Temporal Logic. Both Linear Temporal Logic (LTL) and Computation Tree Logic (CTL) will be studied together with efficient algorithms for model checking formulas in these logics.</p> <p>During the lab a tutorial on NuSMV will introduce the student to one of the most successful software used in industrial applications to specify and test synchronous concurrent systems and critical software.</p>



## SYLLABUS

- Modeling Systems as Transition Systems.
- Temporal Logics:
  - Linear Temporal Logic (LTL)
  - Computation Tree Logic (CTL and CTL\*)
- Model Checking CTL formulas.
- Ordered Binary Decision Diagrams (OBDD's).
- CTL Symbolic Model Checking.
- Model Checking Vs. Proof Theory

## TEACHING FORMAT

Frontal lectures and lab.

## ASSESSMENT

- SMV Project (20%)
- Final Written Exam (80%)

## READING LIST

Text Book:

- Logic in Computer Science--Modelling and Reasoning about Systems. Michael Huth and Mark Ryan. Publisher: Cambridge University Press, 2004.

Additional Reading:

- Model Checking. Edmund Clarke, Orna Grumberg and Doron Peled. Publisher: MIT Press, 1999.

## SOFTWARE USED

- NuSMV

## LEARNING OUTCOME

As a final result of this course, Students will be able to understand the techniques used to specify and verify a hardware component using a formal model checking procedure. Students will be able to understand the meaning of Temporal Logic formulas based on both LTL and CTL and to specify computation properties using such formal languages. Finally, they will be able to use and run the model checker software NuSMV.

## COURSE PAGE

<http://www.inf.unibz.it/~artale/FM/fm.htm>